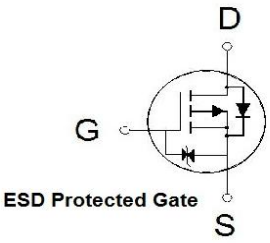
NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

PK5G3EA
PDFN 5x6P
Halogen-Free & Lead-Free

PRODUCT SUMMARY

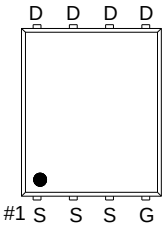
$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	6.1mΩ	-87A



RoHS Compliant

Features
- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated ESD diode with ESD Protected up to 4KV.

Applications
- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



G. GATE
D. DRAIN
S. SOURCE

100% UIS Tested
100% Rg Tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	-87	A
	T_C = 100 °C		-55	
	T_A = 25 °C		-15	
	T_A = 70 °C		-12	
Pulsed Drain Current[1]		I_{DM}	-150	
Avalanche Current		I_{AS}	-68	
Avalanche Energy	L = 0.1mH	E_{AS}	231	mJ
Power Dissipation	T_C = 25 °C	P_D	78	W
	T_C = 100 °C		31	
	T_A = 25 °C		2.3	
	T_A = 70 °C		1.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	$R_{\theta JA}$		55	°C / W
Junction-to-Case	$R_{\theta JC}$		1.6	

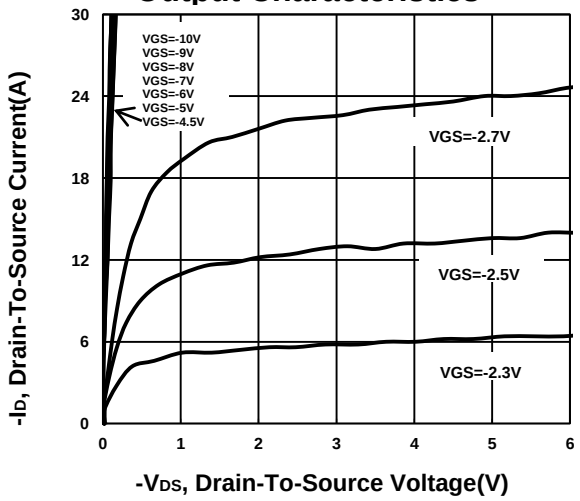
[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

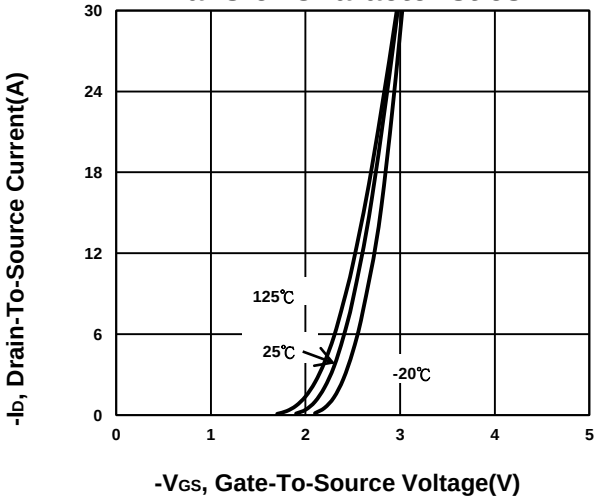
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.3	-1.7	-2.3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	uA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	uA
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -20A		6.5	10.5	mΩ
		V_{GS} = -10V, I_D = -20A		4.1	6.1	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -20A		55		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		4924		pF
Output Capacitance	C_{oss}			795		pF
Reverse Transfer Capacitance	C_{rss}			715		pF
Gate Resistance	Rg	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		1.9		Ω
Total Gate Charge[2]	$Q_{g(VGS=-10V)}$	V_{DS} =-15V, I_D = -20A		120		nC
	$Q_{g(VGS=-4.5V)}$			60		nC
Gate-Source Charge[2]	Q_{gs}			13		nC
Gate-Drain Charge[2]	Q_{gd}			28		nC
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -15V, I_D ≅ -20A, V_{GS} = -10V, R_{GS} = 6Ω		18		nS
Rise Time[2]	t_r			96		nS
Turn-Off Delay Time[2]	$t_{d(off)}$			162		nS
Fall Time[2]	t_f			126		nS
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-60	A
Forward Voltage[1]	V_{SD}	I_F = -20A, V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -20A , dI_F/dt = 100 A / μS		17		nS
Reverse Recovery Charge	Q_{rr}			6.8		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

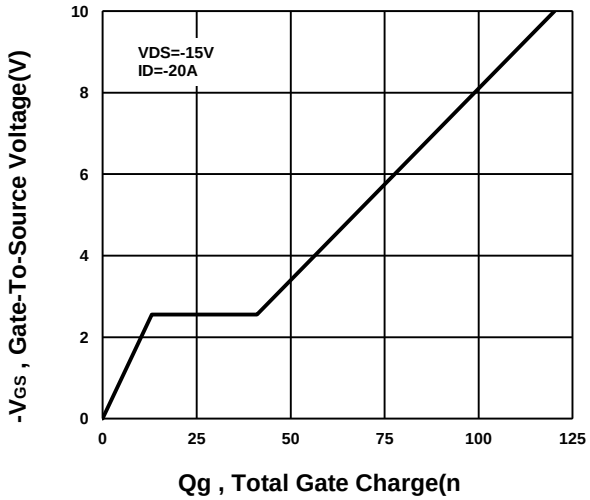
Output Characteristics



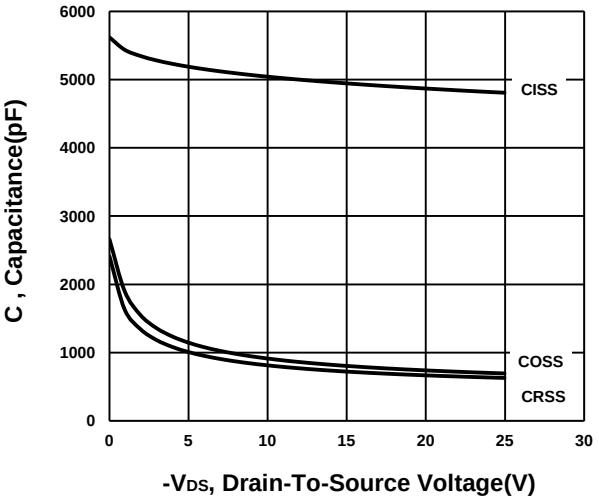
Transfer Characteristics



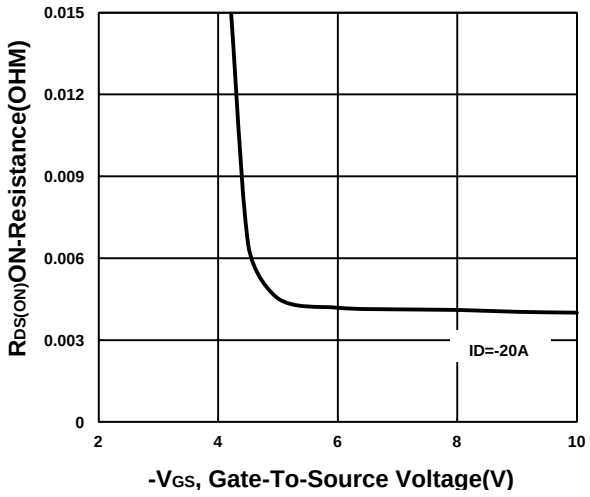
Gate charge Characteristics



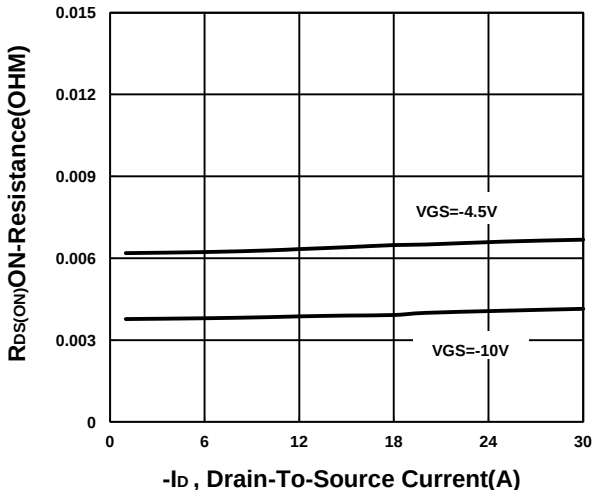
Capacitance Characteristic



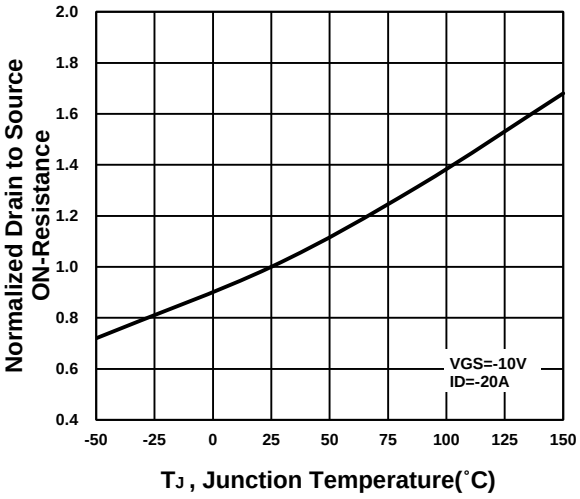
On-Resistance VS Gate-To-Source



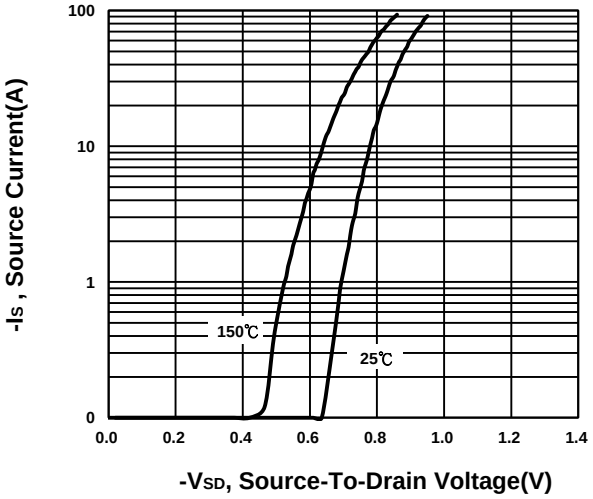
On-Resistance VS Drain Current



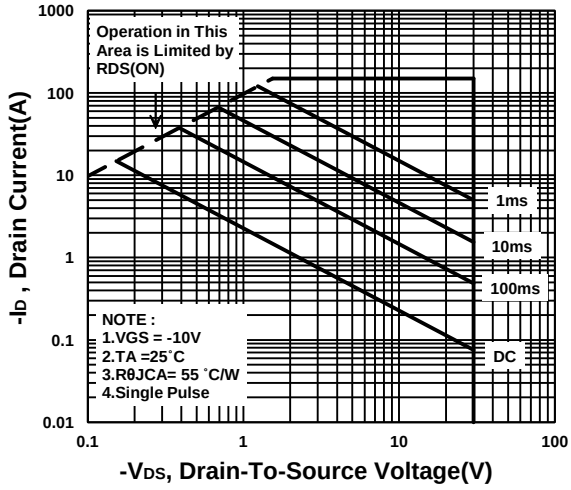
On-Resistance VS Temperature



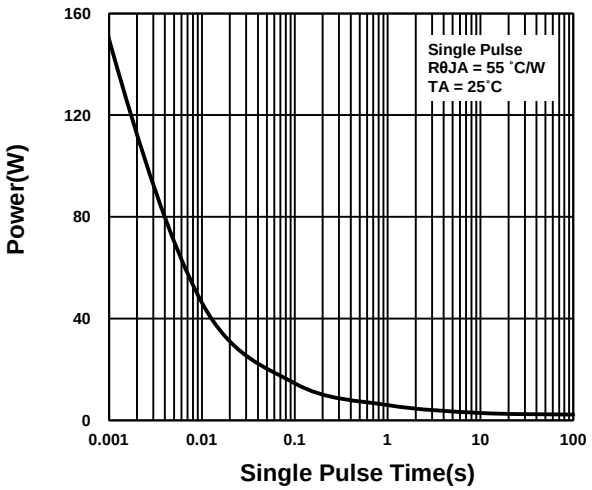
Source-Drain Diode Forward Voltage



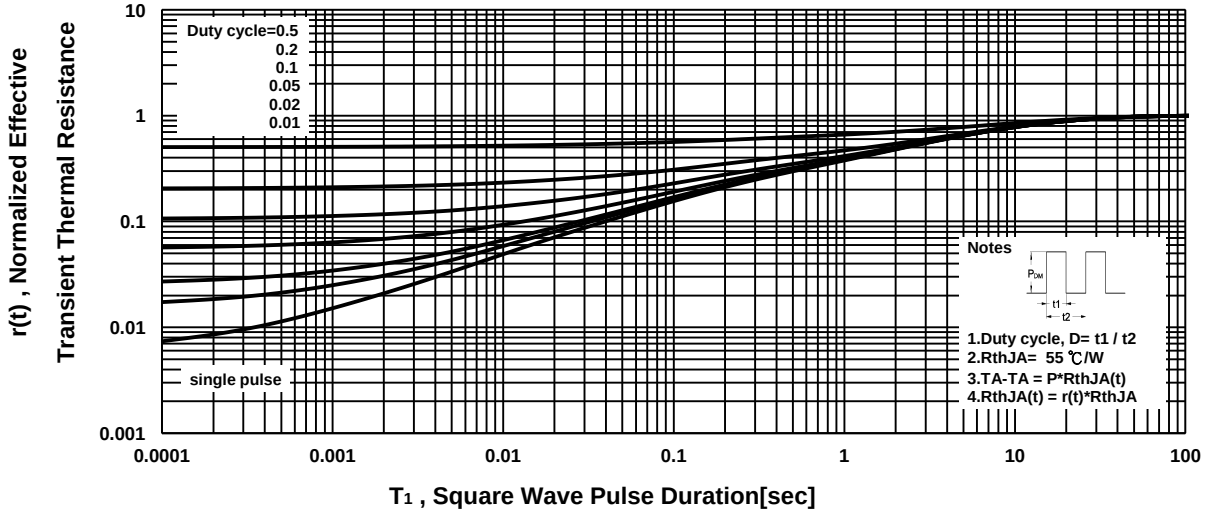
Safe Operating Area



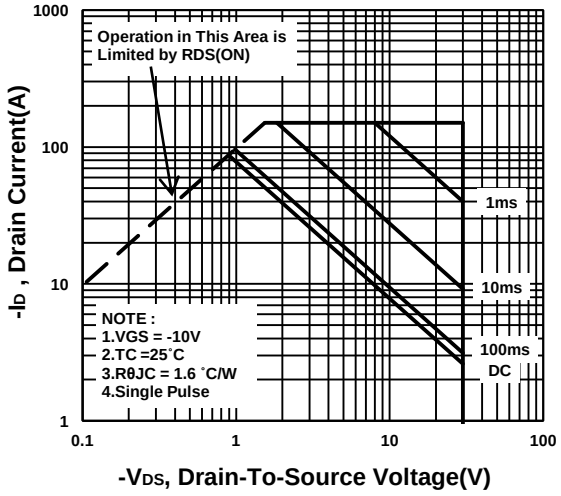
Single Pulse Maximum Power Dissipation



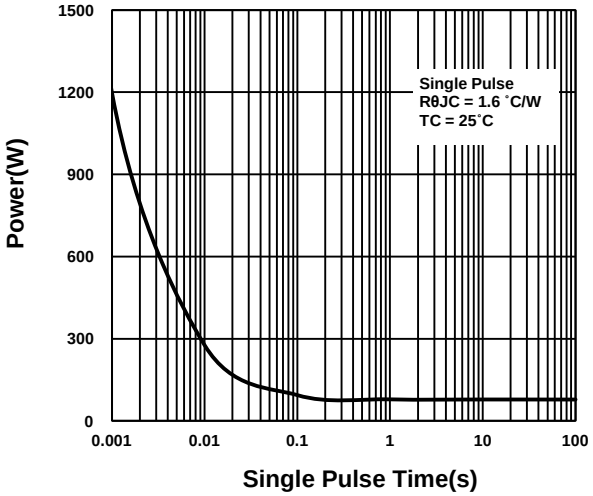
Transient Thermal Response Curve



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve