Low Dropout Voltage Regulator Operation and Performance Review

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Introduction

In today's power management systems, high power efficiency becomes necessary to maximize the lifetime of the battery. Low dropout linear regulators (LDO) have been wildly used in power management due to the characteristics, such as simplicity, low cost, high current density, and small space. This report presents some characteristics of LDO, such as the basic operation, efficiency, line/load regulation, efficiency, etc.

Input-to-Output Dropout Voltage

Dropout voltage is the difference between input and output terminal. Fig. 1 shows an example of an n-channel LDO. N-channel MOSFET is used to simplify the operation introduction; however, n-channel MOSFET devices are not widely used in LDO design.

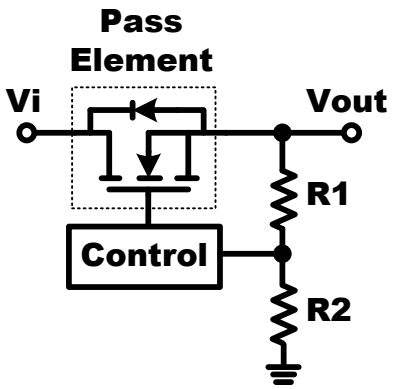


Fig.1. LDO Using N-Channel Pass Element

N-channel MOSFET could operate in two operation region-linear and saturation region. While operating in the saturation region, MOSFET is a voltage control current source, and LDO usually operates in this region. While operating in linear region, MOSFET operates like a resistor. Fig. 2 shows the I-V curve of n-channel MOSFET.

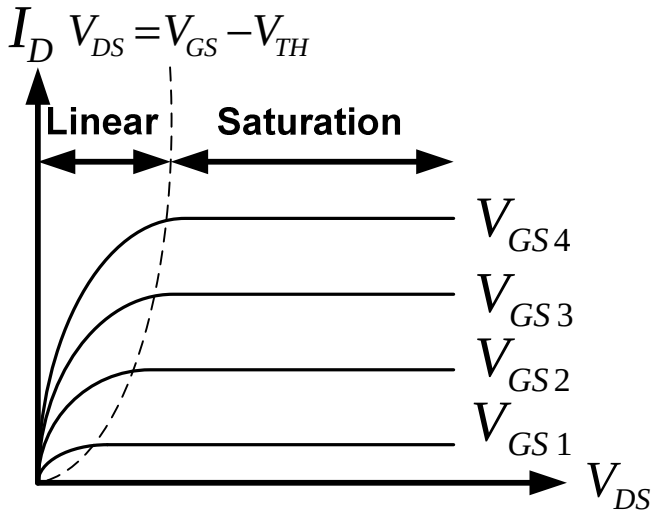
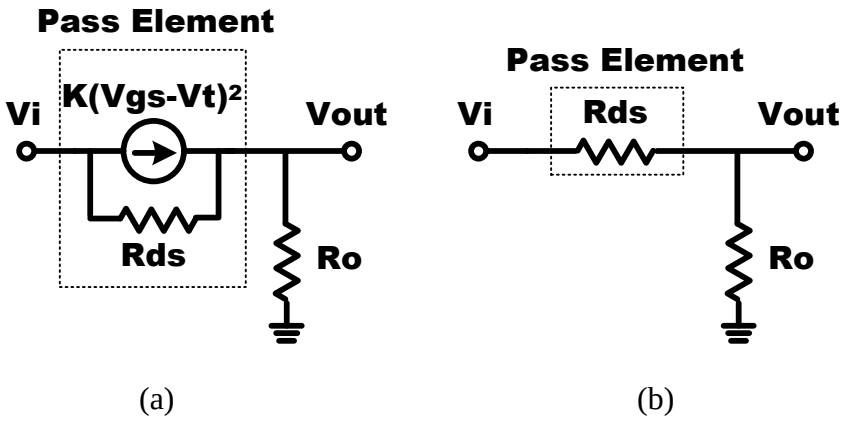


Fig. 2. I-V Curve of N-Channel MOSFET



(a) (b)

Fig. 3. (a) LDO Equivalent Circuit in The Saturation Region
(b) LDO Equivalent Circuit in The Linear Region

Fig.3 shows the equivalent circuit of MOSFET in the linear and saturation region. The saturation current of MOSFET is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs}-V_t\right)^2 \quad (1)$$

where μ_n is the electron mobility, C_{ox} is the parasitic capacitor, and W/L is the width and length ratio of MOSFET. For simplifying, $\frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ is defined as current gain K, so the current of MOSFET is given by

$$I_D = K(V_{gs} - V_t)^2 \quad (2)$$

Under varying load conditions, Vgs voltage controls LDO to keep the output condition in the demand value. Fig. 4 shows the MOSFET operation region as output current increases. When the load current increases form I_{D1} to I_{D2}, the operation point moves from P1 to P2, and if the load current continuously increases, the operation point moves from P2 to P3 locating in the linear region. Fig. 5 shows the MOSFET operation region as input voltage changes. When the input voltage changes from V_{DS1} to V_{DS2}, the operation region is still in the saturation region. If the input voltage decreases from V_{DS1} to $V_{DS3,}$ the operation region changes from saturation region to linear region. Fig. 6 shows the typical LDO operation region. LDO usually operates in three regions: off region, dropout region, and regulation region. If Vin is too small, LDO operates in the off region. If Vin increases but not large enough, LDO can not regulate to the demanded Vout. In this region, it is usually called drop region, and the input voltage is a function of the control loop. When the input voltage still increases, the LDO operates in the saturation region which LDO circuits usually operate in. In this region, the LDO circuit can regulate the output voltage in the demanded value. The dropout voltage is defined as the formula Vin-Vout, and it is the minimum difference between input and output voltage where the circuit ceases to regulate. So the dropout voltage can be expressed in term of a MOSFET resistance.

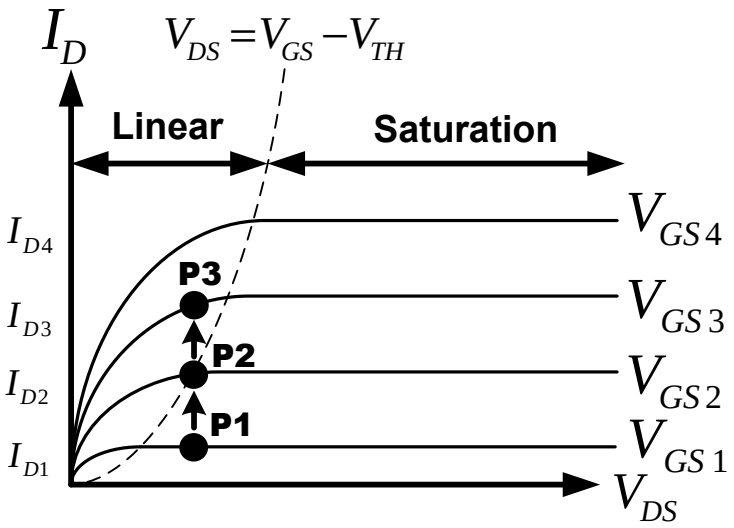


Fig. 4 LDO Using N-Channel MOSFET as Output Current Increases

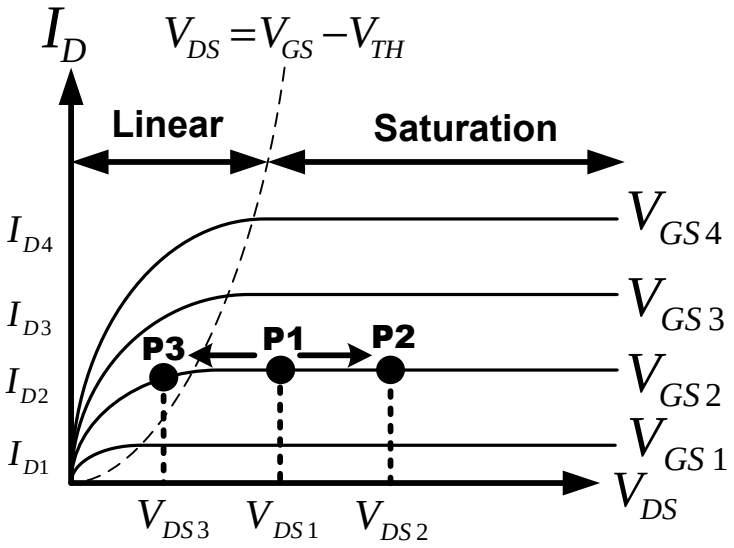


Fig. 5. LDO Using N-Channel MOSFET as Input Voltage Changes

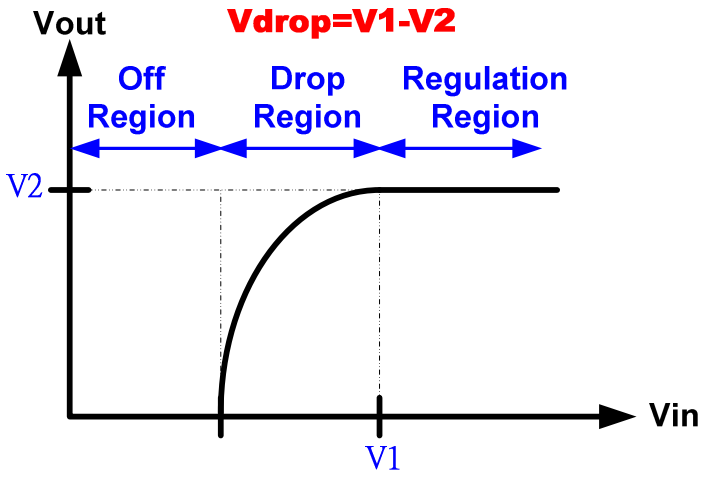


Fig. 6. LDO Operation Region

Ground Current

The ground current is defined as the different between the input current and the out current. Fig.7 shows the ground current of LDO. The ground current consists of the bias current (the band-gap reference, the error amplifier, and the sampling resistors) and the pass element driving current. The ground current is given by

$$I_{ground} = I_{in} - I_{out} \quad (3)$$

If the pass element is BJT transistors, the driving current is larger than the driving current using MOSFETs as pass elements. The driving current of MOSFETs is approximately zero, and the driving current of BJTs is given by

$$I_B = \frac{I_C}{\beta} \tag{4}$$

where I_B is the base current of a BJT, I_C is the collect current of a BJT, and β is the current gain of a BJT. Fig. 8. shows the ground current of a BJT and MOSFET varies with output current. For a BJT, the ground current increases with the output current because a BJT is a current-driven element which is shown in formula (4). For a MOSFET, the ground current is almost constant value while the output current is changed because a MOSFET is a voltage-driven element.

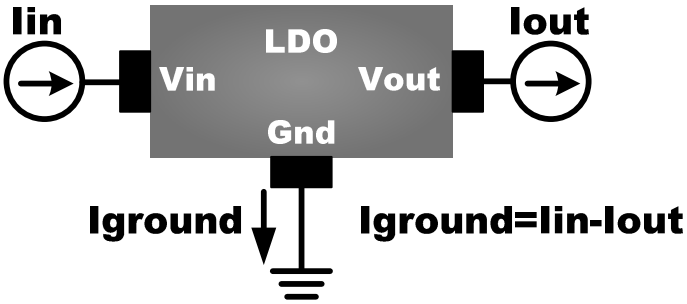


Fig. 7. Ground Current in LDO

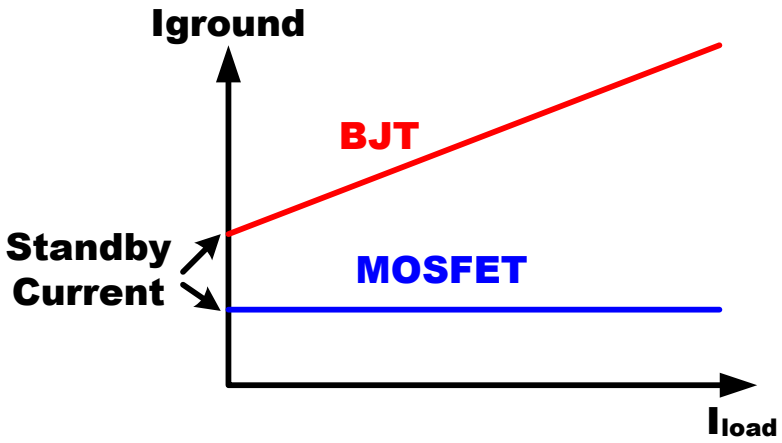


Fig. 8. Ground Current and Output Current

Pass Element Topologies

Fig. 9. shows the five basic pass elements, namely, NPN-Darlington, NPN, PNP, PMOS, and NMOS. The choice of topologies is depend on the process and the application of LDO. The bipolar devices are able to deliver the highest output currents for a given supply. The current capability of MOS transistors is depend on the gate-to-source voltage and the aspect ratio. However, the advantage of MOS transistors is the lowest quiescent current.

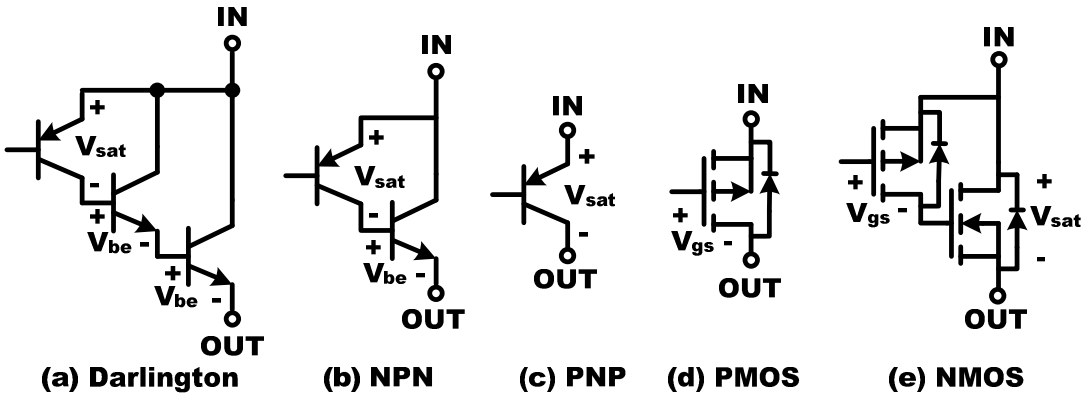


Fig. 9. Pass Element Topologies

The Darlington topology needs at least 1.6V (0.2V+0.7V+0.7V) to regulate to the output voltage; however, the LDO typically operates with 500mV dropout voltage. But this topology has large output current capability. The dropout voltage of this topology is given by

$$V_{(dropout)} = V_{sat} + V_{be} + V_{be} \qquad \text{for Darlington} \qquad (5)$$

The NPN pass element topology is comprised of an n-channel BJT and a p-channel BJT. The drive current of a NPN pass element topology is very small. Because the output current is driven by the base current of the n-channel BJT, and the n-channel BJT is driven by the base current of the p-channel BJT. So the driving current of the NPN topology is very small. The dropout voltage occurs when the p-channel BJT operates in the saturation region. The dropout voltage can be given by

$$V_{(dropout)} = V_{sat} + V_{be} \qquad \text{for NPN Pass Element} \qquad (6)$$

The big advantage of the PNP pass element topology is the very low dropout voltage, but the driving current of this topology depend on the output current is very large. The dropout voltage is given by

$$V_{(dropout)} = V_{sat} \qquad \text{for PNP Pass Element} \qquad (7)$$

For an NMOS pass element, unless a charge-pump is utilized to boost the gate voltage to be larger than input voltage, the dropout voltage is given by

$$V_{(dropout)} = V_{sat} + V_{gs} \qquad \text{for NMOS Pass Element} \qquad (8)$$

A PMOS pass element is typically the best choice yielding a low dropout voltage and low quiescent current. The dropout voltage is given by

$$V_{(dropout)} = I_O \times R_{ON} \qquad \text{for PMOS Pass Element} \qquad (9)$$

Table 1. shows the comparison between the different pass elements on the different features.

Table. 1. Comparison of Pass Element

Parameter	Darlington	NPN	PNP	NMOS	PMOS
I_{O-max}	High	High	High	Medium	Medium
$I_{quiescent}$	Medium	Medium	Large	Low	Low
$V_{dropout}$	$2V_{be}+V_{sat}$	$V_{be}+V_{sat}$	V_{sat}	$V_{gs}+V_{DS}$	V_{SD}
Speed	Fast	Fast	Slow	Medium	Medium

Efficiency

The LDO's efficiency can be defined as a ratio of output power and input power, and it can be given by

$$Efficiency = \frac{I_O V_O}{(I_O + I_{ground})V_{IN}} \times 100 \qquad (10)$$

If neglects ground current, the efficiency is given by

$$Efficiency = \frac{I_O V_O}{I_O V_{IN}} \times 100 = \frac{V_O}{V_O + (V_{IN} - V_O)} \qquad (11)$$

From formula (10) and (11), to get high efficiency, ground current and the dropout voltage should as small as possible.

Load Regulation

Load regulation is a measure of the ability of a LDO to keep to the demanded voltage under varying load conditions. Load regulation is given by

$$Load\_\text{Re}gulation = \frac{\Delta V_O}{\Delta I_O} \tag{12}$$

Fig. 10 shows a load regulation of LDO. When there is a small change of load current, this change will cause output voltage vary. The variable value of output voltage can be given by

$$\Delta V_O = \Delta I_O R_{eq} \tag{13}$$

where Req is the equivalent output resistor seeing from output node (Req=(R1+R2) || Rload≒Rload). The load regulation can be given by

$$\frac{\Delta V_O}{\Delta I_O} = \frac{1}{g_m g_a}\left(\frac{R_1 + R_2}{R_2}\right) \tag{14}$$

All the frequency components are neglected, and the load regulation is a steady-stage parameter. The load regulation is limited by the open loop current gain of the LDO system as shown in the formula (14).

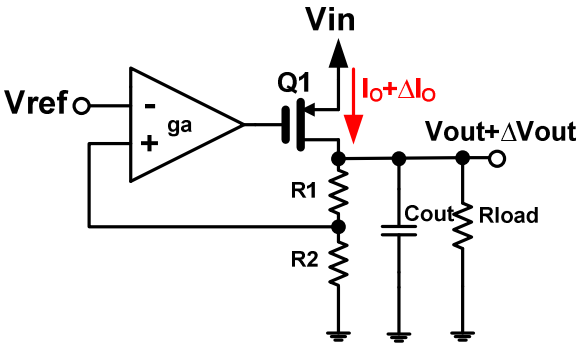


Fig. 10. Load Regulation of LDO

Line Regulation

Line regulation is a measure of the ability of a LDO to keep to the demanded voltage under varying input voltage conditions. Line regulation is given by

$$Line\_\text{Re}gulation = \frac{\Delta V_O}{\Delta V_I} \tag{12}$$

Fig. 11 shows a line regulation of LDO. When there is a small change of input voltage, this change will cause output voltage vary. The variable value of output voltage can be given by

$$\Delta V_O = \frac{R_{load}}{R_{DS} + R_{load}} \times \Delta V_I - \Delta V_O \times \frac{R2}{R1 + R2} \times ga \times gm \times R_{load} \tag{13}$$

$$[1 + \frac{R2}{R1 + R2} \times gm \times ga \times R_{load}] \times \Delta V_{out} = \frac{R_{load}}{R_{load} + R_{DS}} \times \Delta V_I \tag{14}$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{R1 + R2}{R2} \times \frac{1}{gm \times ga \times (R_{DS} + R_{load})} \tag{15}$$

The load regulation and the line regulation are steady state parameters, and the frequency components are neglected. The line regulation can by improved if dc open loop gain increases.

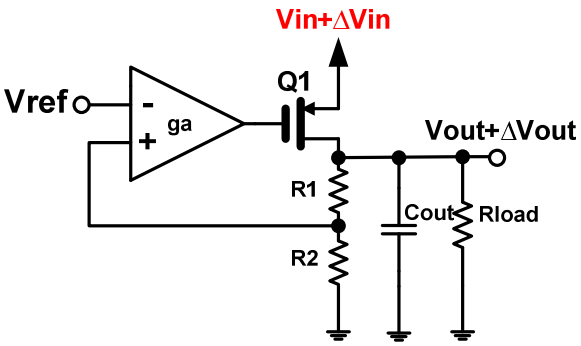


Fig. 11. Line Regulation of LDO

Transient Response

The transient response is the maximum allowable output voltage variation for a load current step change. The transient response is influenced by the bandwidth of LDO, output capacitor, loading current, and the ESR of the output capacitor. Fig. 12 shows the LDO transient response and some time and voltage labels.

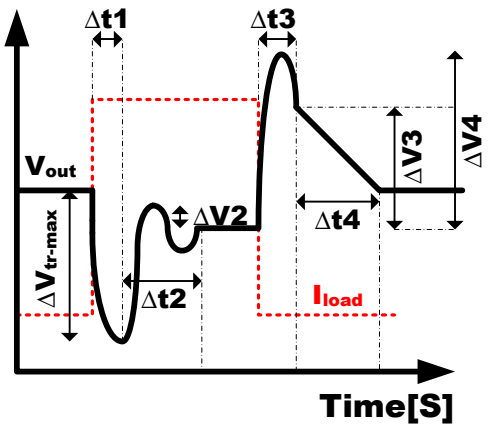


Fig. 12. LDO Transient Response

The worst-case time required for the loop to respond specified by $\Delta V_{tr\text{-}max}$, the maximum permissible output voltage variation, which is a function of the output capacitor, the electrical series resistor of the output capacitor, the bypass capacitor, and the maximum loading current, and it is given by

$$\Delta V_{tr-\max} \approx \frac{I_{load\_\max}}{C_{out}+C_b}\Delta t1 + \Delta V_{esr} \tag{16}$$

$$\Delta t1 \approx \frac{C_{out}+C_b}{I_{load\_\max}}[\Delta V_{tr-\max} - \Delta V_{esr}] \tag{17}$$

where ΔVesr is the variation resulting from the ESR of the output capacitor. The ESR effects can be reduced by the bypass capacitors. In typical implementations, the Δt1 is influenced by the bandwidth and the internal slew-rate associated with the parasitic capacitor of pass element, as shown in Fig. 13.

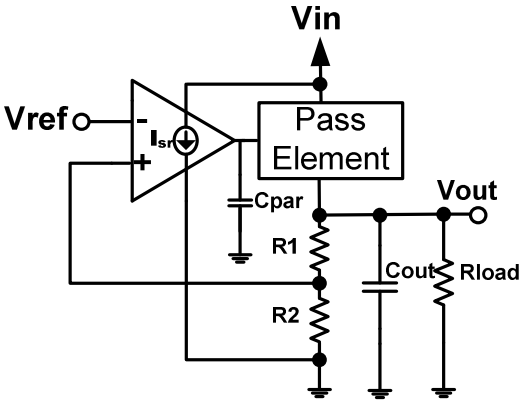


Fig. 13. LDO with Parasitic Elements

The resulting time can be given as

$$\Delta t1 \approx \frac{1}{BW_{close\_loop}} + t_{sr} = \frac{1}{BW_{close\_loop}} + \frac{\Delta V}{I_{sr}} \times Cpar \tag{18}$$

where BW_{close_loop} is the closed-loop bandwidth of the system, tsr is the slew-rate time of the internal operation amplifier, Isr is the slew-rate limit current, and ΔV is the voltage variation at Cpar. If the slew-rate current is large enough, the Δt1 is approximate to the function of the closed-loop bandwidth of the system. Once the slew-rate condition is terminal, the output voltage recovers and settles to the final value as shown in the formula (19).

$$\Delta V_2 = R_{O\_reg} \times I_{load\_\max} \tag{19}$$

where R_{O_reg} is the closed-loop output resistor. The settling time(Δt2) is depend on that the time required for the pass element to fully charge the output capacitor, and the phase margin of the open-loop frequency response. When the loading current pulls down, the output voltage variation peaks at ΔV4, whose voltage magnitude is dominated by the output capacitor charged, and the ESR of the output capacitor. This value can be given by

$$\Delta V4 \approx \frac{I_{load\_\max}}{C_{out} + C_b} \Delta t3 + \Delta V_{esr} \approx \frac{I_{load\_\max}}{C_{out} + C_b} \times \frac{1}{BW_{close\_loop}} + \Delta V_{esr} \tag{20}$$

When the pass element is finally to shut off the variation settles down to ΔV3, the output voltage takes time Δt4 to discharge to its final value. Δt4 is given by

$$\Delta t4 \approx \frac{C_{out}+C_b}{I_{pull-down}}\Delta V3 = \frac{(C_{out}+C_b)R_2}{Vref}\Delta V3 \qquad (21)$$

If the output current is zero, the output capacitor is discharged by the feedback resistor network only.

Frequency Response

To analysis the LDO frequency response, the closed loop network is broken. Fig. 14 shows the LDO small signal equivalent circuit. The error amplifier is modeled by a transconductance (ga), the output equivalent capacitor (Cpar), and the output equivalent resistor (Rpar).

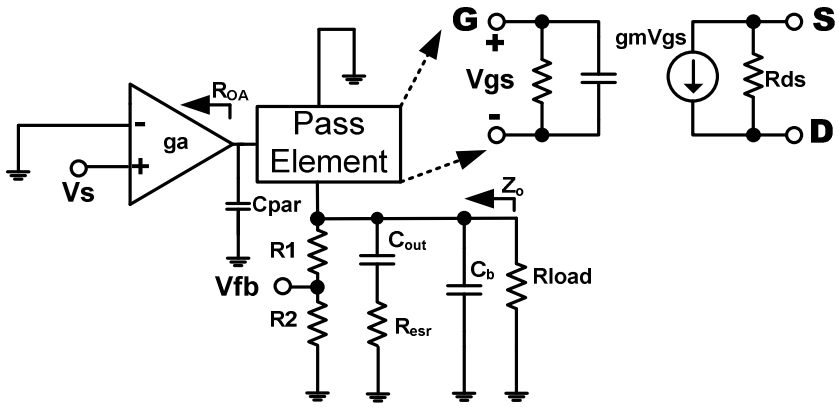


Fig. 14. The Small Signal Equivalent Circuit of LDO

The impedance seeing from Zo is given by

$$Z_O = R_{12P} \parallel (R_{esr} + \frac{1}{SC_{out}}) \parallel \frac{1}{SC_b}$$
$$= \frac{R_{12P}(1+SR_{esr}C_{out})}{S^2 R_{12P}R_{esr}C_{out}C_b + S[(R_{12P}+R_{esr})C_{out}+R_{12P}C_b]+1} \qquad (22)$$

Where R_{12P}=Rds ‖ (R1 + R2) ≒ Rds

The output capacitor is usually larger than the bypass capacitor. So, the impedance seeing form Zo can be approximated to

$$Z_O \approx \frac{Rds(1+SR_{ESR}C_O)}{[1+S(Rds+R_{esr})C_O]\times[1+S(Rds \parallel R_{esr})C_b]} \quad (23)$$

The open-loop gain can be described as

$$\frac{Vfb}{Vs} = \frac{gmaR_{OA}gmZ_O}{[1+SR_{OA}Cpar]} \times \frac{R2}{R1+R2} \quad (24)$$

From the fo4mula (24), the overall open-loop gain of the system is obtained, and the locations of zero and pole are found. The approximated poles and zero can be given by

$$P_1 \approx \frac{1}{2\pi RdsC_{out}} \approx \frac{I_{load}}{2\pi V_A C_{out}} \quad (25)$$

$$P_2 \approx \frac{1}{2\pi R_{esr}C_b} \quad (26)$$

$$P_3 \approx \frac{1}{2\pi R_{OA}Cpar} \quad (27)$$

$$Z_1 \approx \frac{1}{2\pi R_{esr}C_{out}} \quad (28)$$

Where Rds=V_A/I_{load}, V_A is channel length modulation parameter. The locations of poles and zero depend on the architecture of the error amplifier used by the LDO and the type of the output capacitors. Fig. 15 shows the LDO frequency response. Assume the output capacitor (C_{out}) is larger than the bypass capacitor (C_b), so the location of P_1 is very small than the location of P_2. To maintain the stability of the LDO circuit, the location of Z_1 is used to cancel the effect of P_3, and the location of P_2 is placed to be larger than the unit-gain bandwidth.

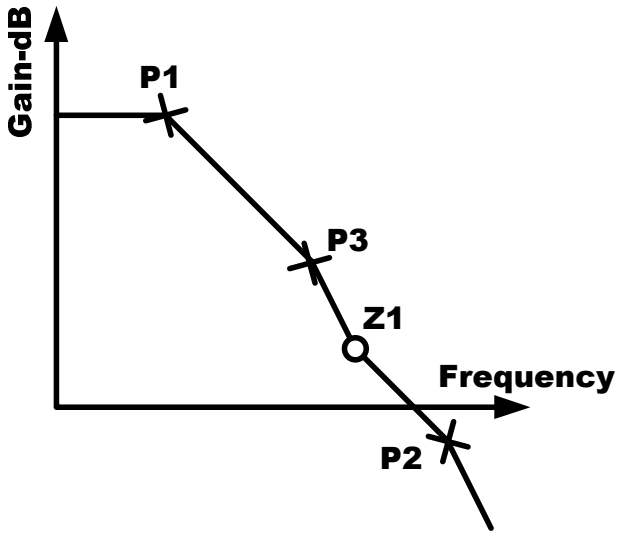


Fig. 15 Frequency Response of LDO

Range of stable ESR (Tunnel of Death)

A typical LDO regulator requires an output capacitor with an equivalent series resistor (ESR) to maintain in the stabilization. A LDO typically has two poles before unity gain bandwidth, and these poles without compensation could cause oscillation as shown in Fig. 16.

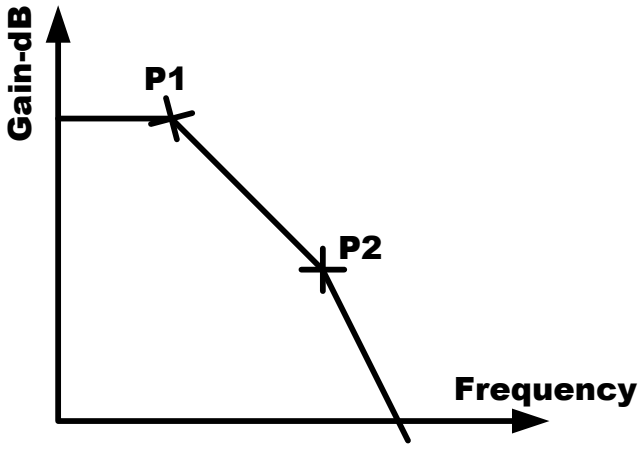


Fig. 16 LDO Frequency Response without Compensation

The equivalent series resistance of the output capacitor is used for generating a zero. This zero produced by the ESR is placed before the unity gain frequency (UGF) so that the phase shift will be compensated. Therefore, the linear regulator is stable because there is only one effect pole in the left side of UGF as shown in Fig. 17.

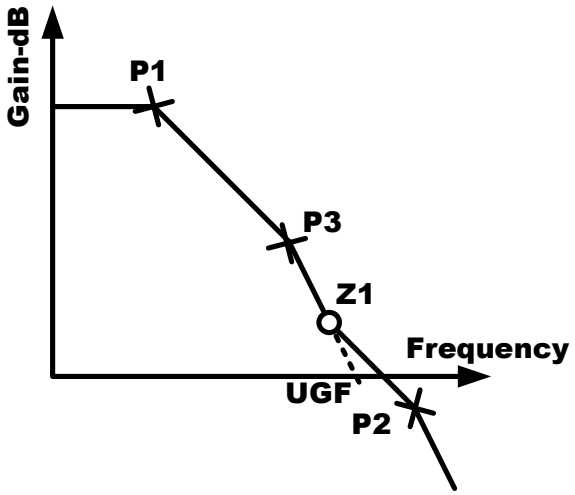


Fig.17 Frequency Response with Compensation

The ESR value must be maintained in the range that determines the loop stability. Fig. 18 and Fig. 19 show that the zero compensated by ESR is out of the range. If the value of ESR is too low, the compensated zero will be placed at the high frequency, and there are still two poles in the left side of UNF as shown in Fig. 18.

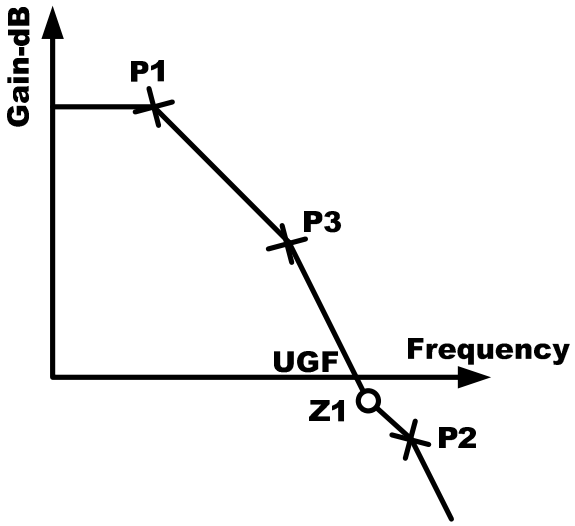


Fig. 18 Unstable Condition While the Zero in the High Frequency

If the value of ESR is too large, the compensated zero will be placed at the low frequency, and another pole (P3) appears in the left side of UGF, and even there is a zero, there are still two effect poles in the left side of UNF as shown in Fig. 19.

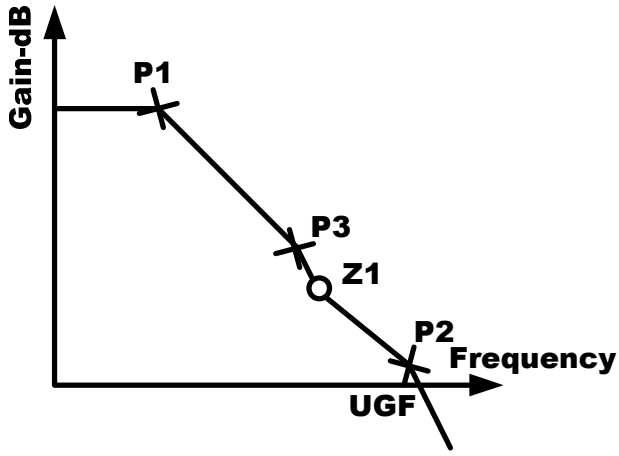


Fig. 19 Unstable Condition While the Zero in the Low Frequency

Because ESR can cause instability, a range must be provided to show the stable values of ESR. Fig. 20 shows a typical range of ESR values with respect to the output currents.

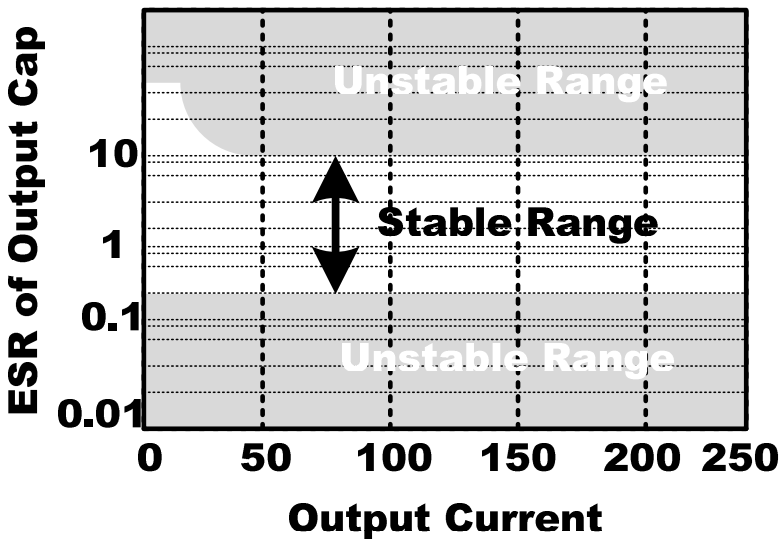


Fig. 20 Range of Stable ESR Value

Reference

[1] Gabriel Alfonso Rincon-Mora, “Current Efficient, Low Voltage, Low Drop-Out Regulators,” Ph.D Thesis, Georgia Institute of Technology, November 1996.
[2] Texas Instruments, “Technical Review of Low Dropout Voltage Regulator Operation and Performance,” Application Report, August 1999.